Use of Series Connected SiC Devices in a 2 x 330kW, 1500Vdc Power Converter design

Peter J R Allan, Paulo J Torri*

Turbo Power Systems, Gateshead, United Kingdom
Pallan@turbopowersystems.com
**Ptorri@turbopowersystems.com*

Keywords: Sillicon Carbide, Series Connection, Snubber, de-saturation, Short Circuit

Abstract

Silicon Carbide (SiC) MOSFET's allow for higher switching frequencies in power converters leading to smaller filter components and increased power density. Commercially available packages capable of handling high voltages are limited. Multilevel converter topologies can be used to accommodate lower voltage devices but can add complexity to the overall converter design. This paper explores the use of series connected 1200V 300A SiC MOSFET's with a conventional two-level inverter configuration. Voltage sharing between series connected devices is explored through double pulse tests. A passive method of gate driver trimming is presented to optimise voltage sharing. The work also discusses short circuit protection, busbar and snubber design. Voltage sharing is validated through running the converter at high temperature. Turn-off transitions are well matched. Challenges in matching the opposite device's diodes during switching was identified as a subject for future work.

1 Introduction

This work presents the test results of a Power Electronic Device (PED) based on series connected SiC MOSFET's to be used in a Medium Voltage (MV) grid connected power converter. The converter will connect two neighbouring substations (11 kV rated voltage) and is referred to as the Soft Power Bridge (SPB). A simplified block diagram of the SPB is shown in Fig. 1:

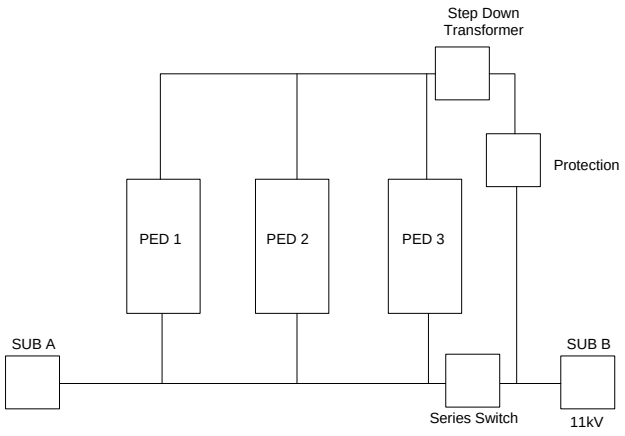

Fig. 1. SPB Block Diagram

The SPB consists of three PED converters working with a DC link voltage of 1500V and rated to 2 x 330kW of power each. To handle the high DC link voltage, series connected SiC MOSFET's are used. Active methods of optimising voltage sharing of these devices has been explored in literature[1]. This work presents a passive method of optimising voltage sharing. Each PED converter consists of an input stage that converts three phase AC to a DC bus and a secondary stage that converts the DC voltage to a single phase AC output used to control the flow of active and reactive power between two substations. A power stage diagram of the PED is shown in Fig. 2:

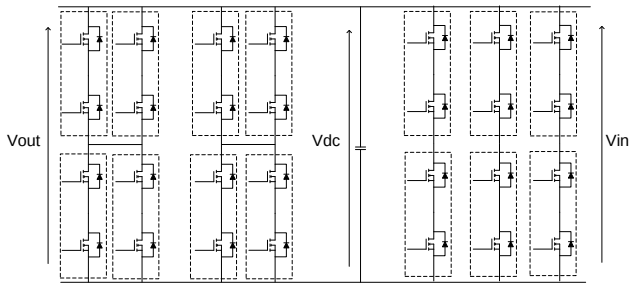

Fig. 2. PED Power Stage Diagram

The PED is designed as a two-level converter[2]. The SPB is designed to help with greater utilisation of the existing power network to accommodate increasing demands. Topics covered in this paper focus on voltage sharing of SiC devices in series connection through correct gate driver trimming and snubber design for static and dynamic balancing [3]. Short circuit protection is also investigated[4]. The SPB is part of an UKPN innovation project (Active Response), partially funded by OFGEM[5].

2. Power Electronic Device (PED)

The PED is designed around a low inductance DC busbar. This reduces over voltages and extra losses on each device during turn-off. Snubbers are designed to reduce any over voltage during turn-off and to help balance the series switching transitions. Equal gate driver channel delays between series connected devices are achieved through careful PCB layout and correct selection of components. Channels are further

trimmed to negate non linearities in devices and components ensuring balanced turn-on/off times. Finally, the protection by de-saturation scheme is optimized for the shortest detection time possible without false tripping.

2.1 PED Specification

The specification for the PED converter is shown in Table 1. The PED can provide 330kW of bidirectional power. 1.2kV SiC MOSFET devices are used in series to handle the full 1500V DC link. A low busbar inductance with careful snubber and gate driver design help the PED utilise series connected devices.

PED Specification	
Power	330kVA
Input Voltage 3Ø	850Vrms
Input Current 3Ø	204Arms
Output Voltage 1Ø	1100Vrms
Output Current 1Ø	300Arms
Line Frequency	50Hz
Switching Frequency	20kHz
DC Bus Voltage	1500V
Cooling	Water Cooling

Table 1 PED Specification

2.2 Snubber Design

The snubber circuit is designed to address three main properties of the MOSFET during switching which is the overvoltage during turn-off and the static and dynamic balancing of the device. The static balancing is defined as how well the two series connected devices share voltage when they are off. This is addressed using resistive dividers in parallel with each device. The dynamic balancing acts when the device is transitioning from on to off. This is to be mainly addressed by an optimized gate driver design and helped by an RC circuit in parallel with each device. An RCD snubber limits the overvoltage seen by the device during turn-off. The complete snubber circuit is shown in Fig. 3.

2.2.1 RC Snubber: The turn-off time for the SiC MOSFET is 100ns. This value is selected as the time constant for the RC Snubber. C_d is chosen to be a small value of 220pF:

$$R_d = \frac{100ns}{220pF} \approx 470\Omega \tag{1}$$

2.2.2 Static Balancing Circuit: For static balancing, resistors are included across each device. The value can be sized based on the device leakage current. The total resistance R_s across each device was selected as 400KΩ.

2.2.3 DC Clamp RCD Snubber: The initial design parameter for the DC bus inductance was between 40-80nH. The estimated busbar inductance is calculated in 3.1. The RCD snubber limits the overvoltage produced by this inductance during turn-off. The energy is instead transferred from the inductance to the snubber:

$$\frac{1}{2}LI^2 = \frac{1}{2}C\Delta V^2 \tag{2}$$

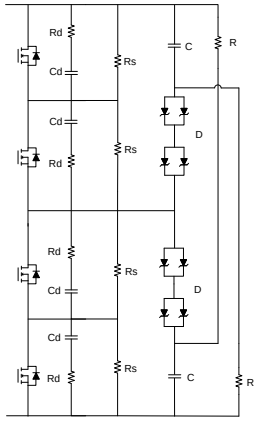

Fig. 3. Snubber Schematic

The equation can be solved to determine the maximum overshoot during turn-off:

$$\Delta V = I_{PK}\sqrt{\frac{L}{C}} \tag{3}$$

A good design should limit the overvoltage to 200V giving a capacitor value of around 470nF. The capacitor must discharge before the next turn-off. The switching period is 50us. The capacitor takes around 5 time constants to discharge fully. The resistor can be calculated as:

$$R = \frac{10us}{470nF} \approx 22\Omega \tag{4}$$

2.3 Gate Driver, De-saturation and Short Circuit

2.3.1 Propagation Delay: Interface cards accommodate the gate driver connection to each module. One interface card holds two dual channel gate drivers. Interface cards were developed to ensure an even propagation time between both series devices. The delay on each channel from issuing a turn-on pulse to when it reaches the device is around 500ns. This is important to know for design of the control loop and to have very low consistent time delays between each gate driver channel.

2.3.2 De-saturation Circuit: The de-saturation circuit is used to detect a short circuit event on the device. As the current exceeds the devices rated current, the voltage of the device begins to increase. Once a specified threshold is reached, a comparator indicates a fault to the microcontroller and switching is stopped. This type of circuit has been used extensively for IGBT devices. The circuit is shown in Fig. 4.

2.3.3 Short Circuit Detection: The blanking time is determined by the ratio of R1, R2 and Cn. Cn also serves to filter noise from the comparator pin and reduce the likelihood of false tripping. IGBT's switch slower than SiC devices and protection can be affective with longer blanking times. When

using this circuit with SiC MOSFET's, the blanking time must be minimised. To reduce the blanking time, the resistor R2 must be reduced. This reduces the time to activate the protection, but also reduces the final trip threshold. The minimum trip voltage is limited by the voltage drop of the DESAT diode and a small voltage offset created by the isolated power supply of the gate driver. When these values are too close, false tripping can occur during normal operation.

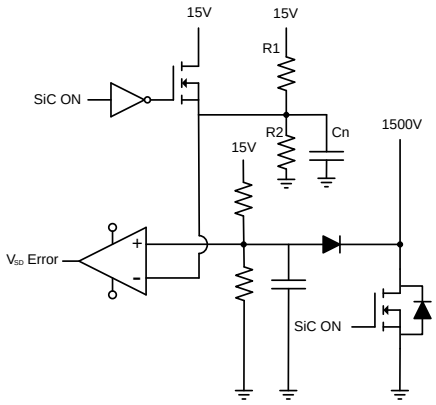

Fig. 4. Classical De-saturation Circuit [6]

2.4 Double Pulse Testing of series connected devices

Initially, inverter legs are fitted with identical turn-off resistor values. Each leg is pulsed individually to determine the voltage imbalance between series devices. Gate resistor values are then trimmed to find the best voltage balancing compromise without compromising switching performance. The device with the slowest turn-off will assume less of the DC bus voltage. The gate resistance of the slowest device is reduced and the test is repeated until voltage sharing is optimal. This process is repeated for each leg of the converter. Once complete, the components of a leg are matched. Fig. 6 shows the imbalance in an initial test. The purple voltage trace shows the quickest device holding most of the voltage. Decreasing the gate resistance of the second device (blue voltage trace) speeds up the switching transition. Fig. 7 shows the final results of this trimming process, with a very good voltage balance between both series connect devices.

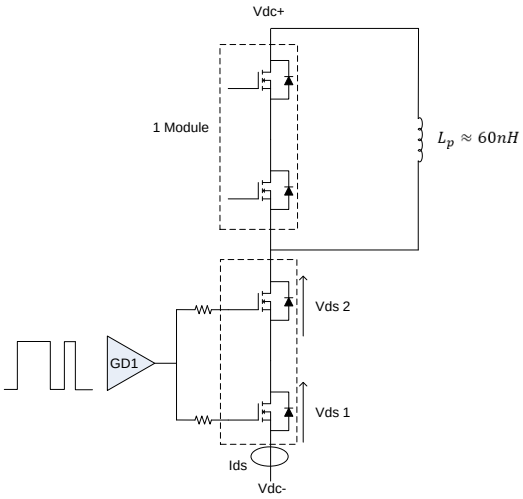

Fig. 5. Double Pulse Test Circuit

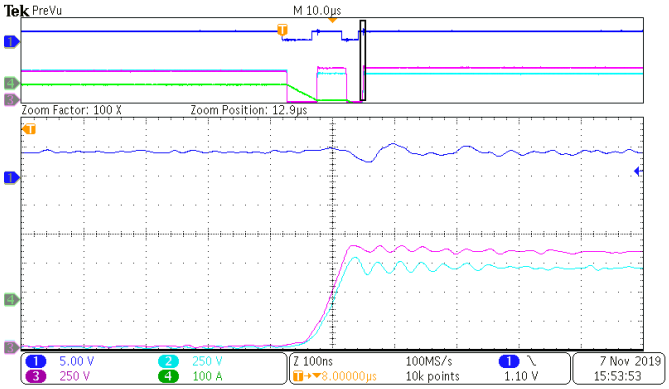

Fig. 6. Series connected devices with voltage imbalance. (Gate Drivers not trimmed). Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time 100ns/div

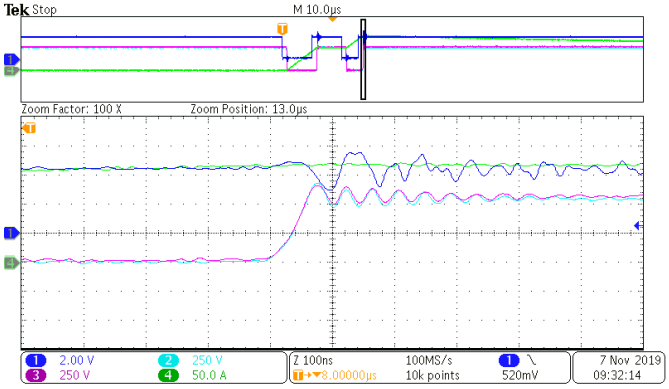

Fig. 7. Phase Leg series connected devices with voltages well balanced (Gate Drivers trimmed). Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 50A/div, Time 100ns/div

3 PED assembling and Test Results

A PED prototype converter shown in Fig. 8 has been built and used to validate the design.

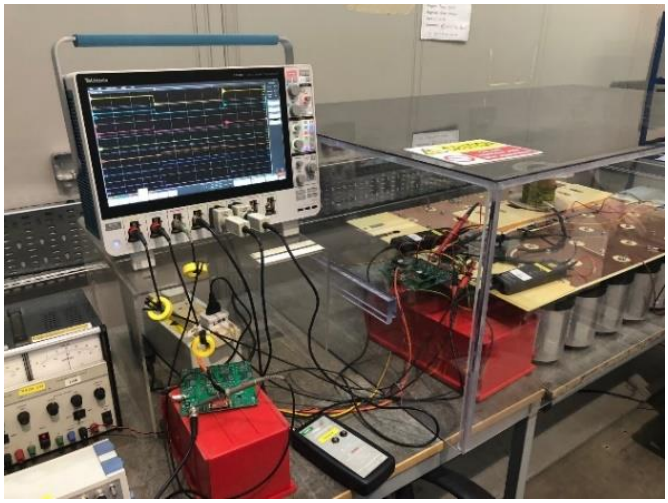

Fig. 8. PED Converter Prototype

3.1 Busbar Inductance Measurement

The busbar inductance is calculated from the double pulse waveforms shown in Fig. 9. As the bottom device turns on, the current through the load freewheels through the anti-parallel diode of the top device which creates a temporary short circuit at which point the inductance of the busbar can be estimated as:

$$L_{bus} = V\frac{dt}{di} = 200 \times \frac{100ns}{600A} = 33nH \qquad (5)$$

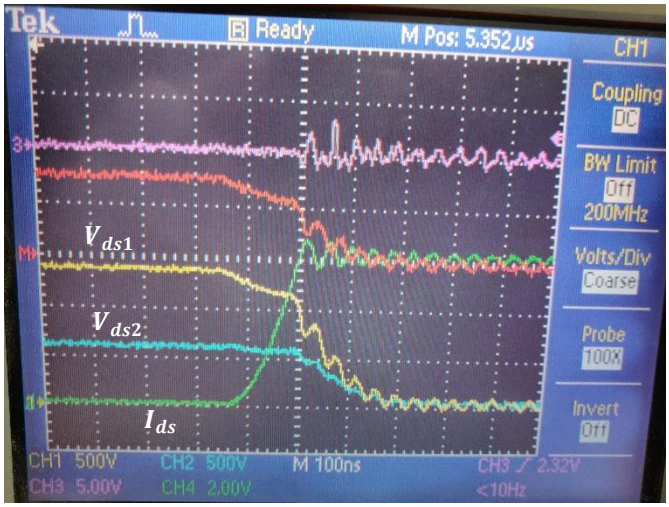

Fig. 9. Busbar inductance during freewheel. Ch1 – V_{ds1} 500V/div, Ch2 - V_{ds2} 500V/div, Ch4 - Device Current I_{ds} 200A/div, Time 100ns/div

3.2 Snubber Test Results

The snubber circuit helps reduce the overvoltage and losses seen by the device. Fig. 10 shows the turn-off transition with no snubber, the overvoltage is above 1kV and peak switching losses are around 400kW. The improvements of using the snubber are shown in Fig. 11 which show that the overvoltage is now limited below 1kV and switching losses are reduced to a peak of 200kW.

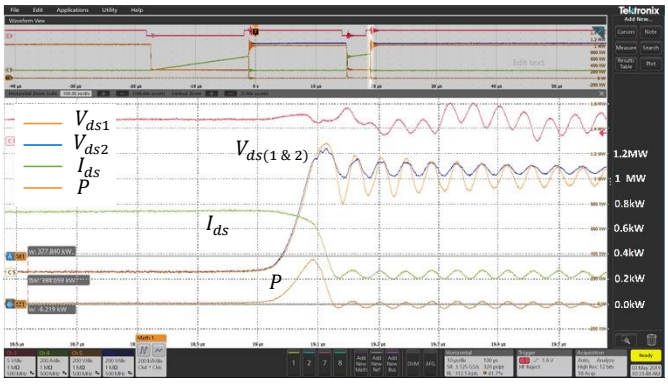

Fig. 10 Switching power losses with no Snubber. Ch5 – V_{ds1} 200V/div, Ch6 - V_{ds2} 200V/div, Ch4 -Device current I_{ds} 200A/div, Time 100ns/div

3.3 De-saturation and Short Circuit

The de-saturation circuit protects the device during a short circuit fault. The short circuit detection time has been

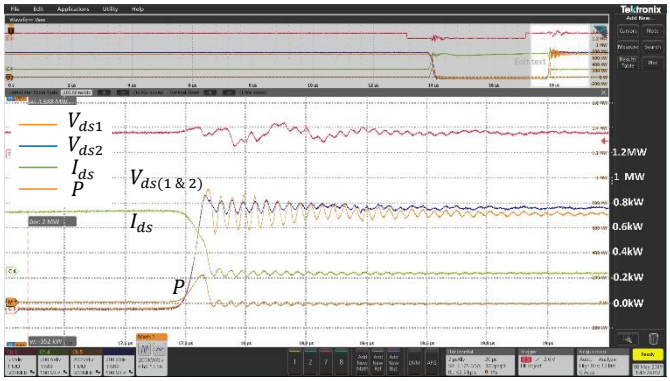

Fig. 11 Switching power losses with Snubber. Ch5 – V_{ds1} 200V/div, Ch6 - V_{ds2} 200V/div, Ch4 - Device Current I_{ds} 200A/div, Time 200ns/div

optimised. If the turn-on pulse is short enough, the protection may not activate, and the device may suffer a "hard" commutation. Good busbar design and snubber design can help in this situation. To validate the circuit, a short is placed across two series connected devices in place of the double pulse inductor shown in Fig. 5. The voltage is measured across each device. The protection is tested above the rated DC link voltage with the result shown in Fig. 12. Protection is activated after 1.2uS and the circuit performs a "soft" turn-off. Both devices survive and don't exceed their rated voltage. This gives good confidence in the final design. A voltage imbalance behaviour between the devices is observed during a short-circuit which could be investigated further.

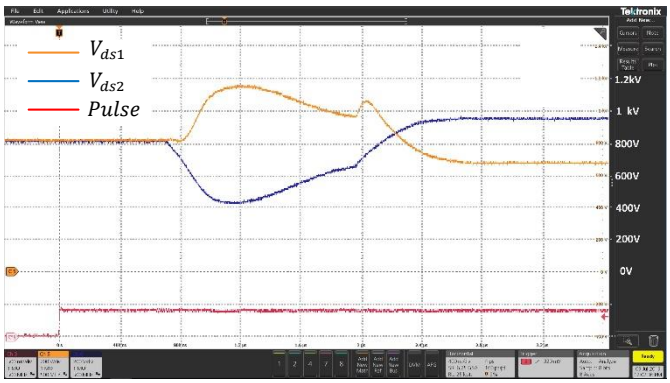

Fig. 12. Short circuit condition at 1600V series connection. Ch3 – Turn-on pulse 5V/div, Ch5 - V_{ds1} 200V/div, Ch6 - V_{ds2} 200V/div, Time 400ns/div

3.4 Voltage Sharing of Series Devices

After each inverter leg has been trimmed, the input converter is then operated at the rated voltage of 1500 Vdc with sinusoidal output current. The test setup is shown in Fig. 13 and waveforms in Fig. 14. It can be seen that voltage sharing is good between devices during the positive half cycle. This is when current is flowing through the MOSFET with turn-on and turn-off transitions shown in Fig. *15* and Fig. *16* respectively. This behaviour was optimised during the double pulse tests. Voltage sharing begins to drift apart during the negative half cycle when the diodes are conducting. Fig. *17* and Fig. *18* show turn-on and turn-off behaviour where voltage

sharing is seen to be not good. Finally, Fig. 19 and Fig. 20 confirm that voltage sharing remains good at temperatures of 120°C.

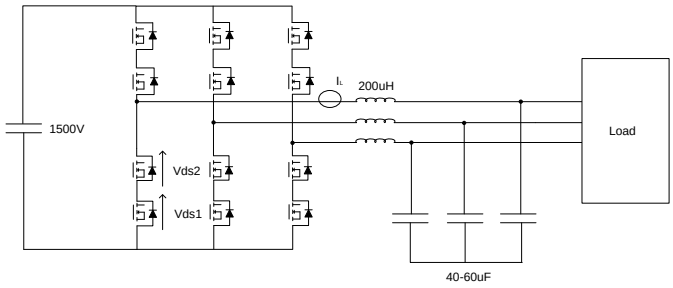

Fig. 13. PED Test Setup

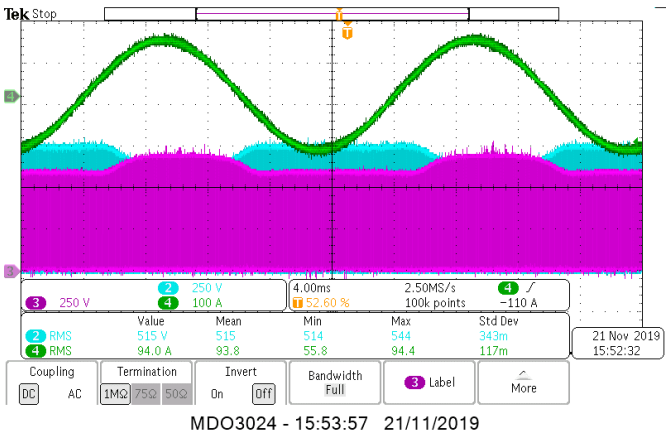

Fig. 14. PED test results. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_L 100A/div, Time 4ms/div

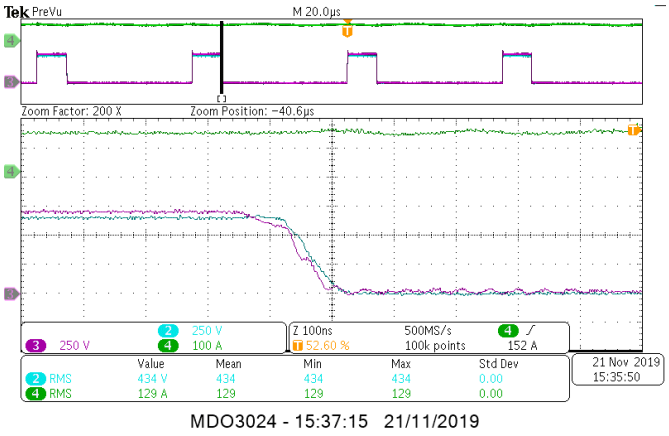

Fig. 15. Device turn-on 20°C positive current. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time 100ns/div

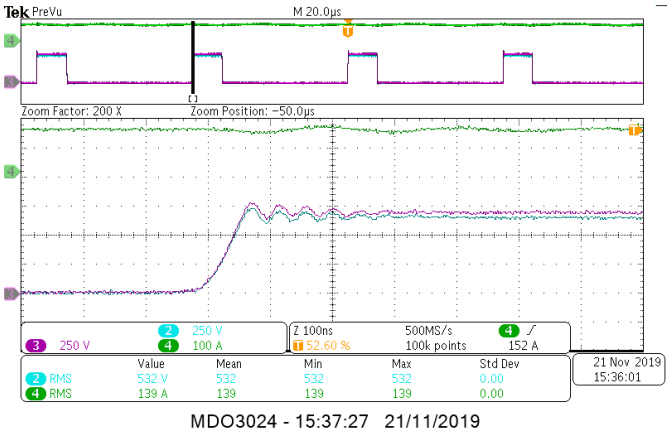

Fig. 16. Device turn-Off at 20°C positive current. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time *100*ns/div

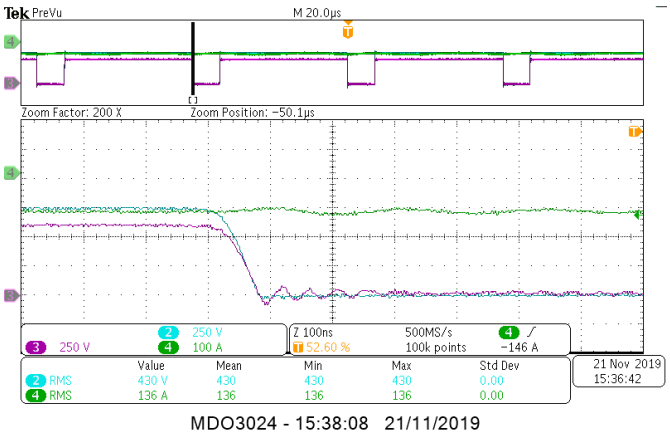

Fig. 17. Device turn-on negative cycle 20°C. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time *100*ns/div

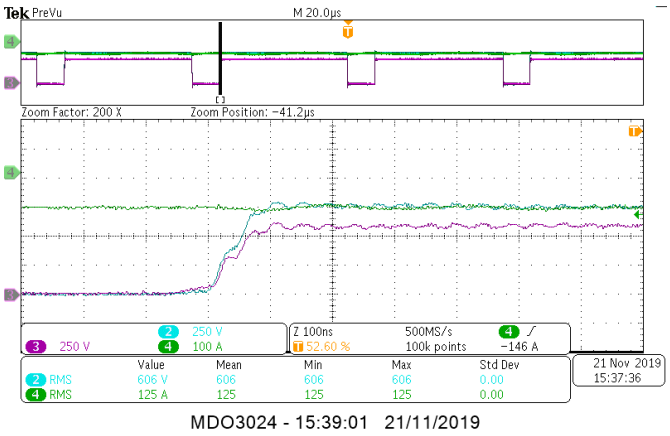

Fig. 18. Diode during turn-off 20°C. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time 100ns/div

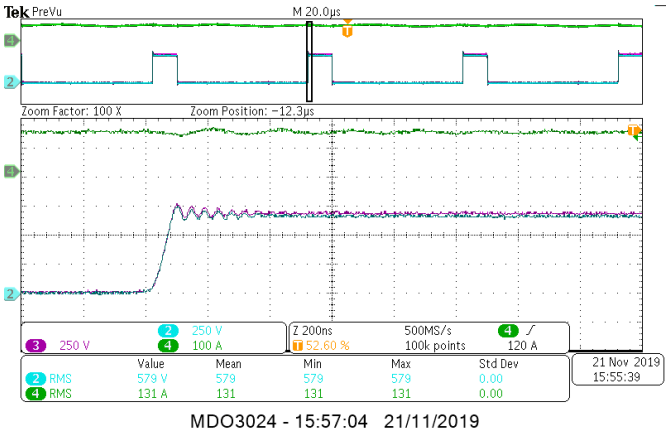

Fig. 19. Device turn-off At 120°C. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time 200ns/div

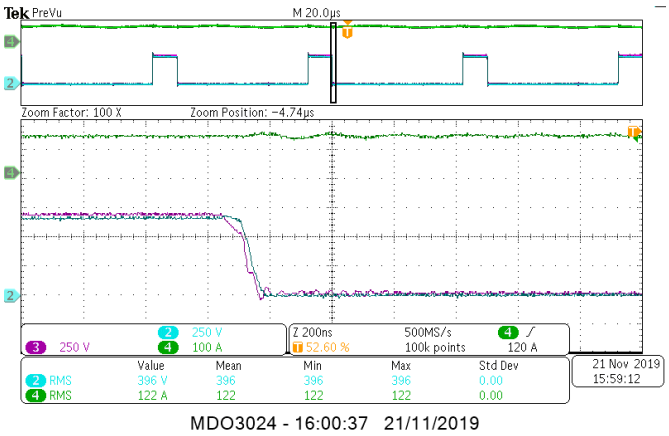

Fig. 20. Device turn-on 120°C. Ch2 – V_{ds1} 250V/div, Ch3 - V_{ds2} 250V/div, Ch4 - Device current I_{ds} 100A/div, Time 200ns/div

4 Conclusion

A power converter has been designed and validated based on a two level topology using series connected SiC MOSFET's. The problem of sharing voltage between series connected devices has been investigated. It was found that small variations in turn-off time can lead to large variations in the devices sharing voltage. A method of passively balancing these devices through gate driver trimming was proposed and tested through double pulse tests at rated voltage and current. Voltage sharing was also validated with success at high temperature. Short circuit tests were performed on series connected devices. Both devices survive short circuit conditions above the rated DC bus voltage, validating the design. Some imbalance behaviour was observed during short circuit conditions which could be investigated further. The potential to balance diode behaviour during switching is also highlighted as possible future work. Busbar, gate driver and snubber design aspects are also discussed and validated to help with series connection of devices.

5 References

[1] K. Wada and K. Shingu, "Voltage Balancing Control for Series Connected MOSFETs Based on Time Delay Adjustment Under Start-Up and Steady-State Operations," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 5495-5499, doi: 10.1109/ECCE.2018.8557461.

[2] S. Hazra, S. Madhusoodhanan, G. K. Moghaddam, K. Hatua, and S. Bhattacharya, "Design Considerations and Performance Evaluation of 1200-V 100-A SiC MOSFET-Based Two-Level Voltage Source Converter," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4257-4268, 2016, doi: 10.1109/TIA.2016.2587098.

[3] X. Yuan, N. Oswald, and P. Mellor, "Superjunction MOSFETs in Voltage-Source Three-Level Converters: Experimental Investigation of Dynamic Behavior and Switching Losses," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6495-6501, 2015, doi: 10.1109/TPEL.2015.2434877.

[4] J. Person, M. Andresen, T. Rettmann, O. Muehlfeld, and M. Liserre, "Short Circuit Detection Methods for Silicon Carbide (SiC) Power Semiconductors," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 7-9 May 2019 2019, pp. 1-7.

[5] 2020. [Online]. Available: https://innovation.ukpowernetworks.co.uk/projects/active-response/.

[6] J. Krapp, "Technical Explanations SKYPER® 42 LJ," 2017. [Online]. Available: www.semikron.com.